1. General Description

ARF4501 is an integrated high power front end module (FEM) designed for Wi-Fi 6 (802.11ax) systems. The compact form factor and integrated matching minimizes layout area in the application. The ARF4501 port impedance is 50 Ω.

2. Features

5 V Operation

31dB TX Gain

14dB RX Gain

MCS11, +18 dBm, -43 dB EVM

MCS9, +22.5 dBm, -35 dB EVM

MCS7, +23.5 dBm, -30 dB EVM

16Pin 3X3mm QFN Package

Integrated 802.11ax, 5 GHz PA, LNA with bypass, and T/R switch

Integrated logarithmic power detector and directional coupler

3. Applications

802.11ax set-top boxes, networking, and personal computer systems

Mini-cards & half mini-cards

Wi-Fi Media Gateways

Consumer Electronics

PC cards, PCMCIA,

Access Points / Routers

Set Top Boxes / Wireless IPTVs

Other 5GHz ISM Platforms

4. Functional Block Diagram

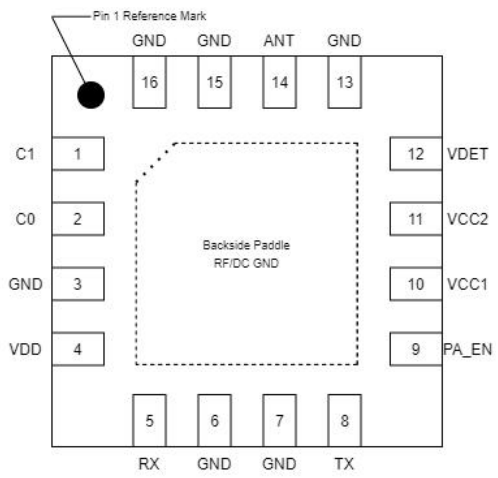


Figure1.

5. Order product model

ARF4501

Directory

6. Specifications

6.1. Electrical Specifications

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

Table1. Transmit Mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Frequency Range			5.15		5.85	GHz
Gain	G		30	31	31.5	dB
Gain flatness	ΔG	Over any 160 MHz band	-1		1	dB
		Over any 80 MHz band	-0.5		0.5	dB
Output power	POUT	MCS11, HE160, DEVM = -43 dB		18		dBm
		MCS11, HE160, DEVM = -40 dB		20.5		dBm
		MCS9, VHT160, DEVM = -35 dB		22.5		dBm
		MCS7, HT40, DEVM =-30 dB		23.5		dBm
		MCS0, HT20, mask compliant		25.5		dBm
Current consumption	ITOT	@ +25 dBm		430		mA
		@ +22 dBm		330		mA
		@ +20.5 dBm		300		mA
		@ +18.0 dBm		280		mA
2nd harmonics	2fo	+25 dBm MCS0		-25		dBm/MHz
3rd harmonics	3fo	+25 dBm MCS0		-30		dBm/MHz
non-harmonic spurious		+25 dBm MCS0		-45		dBm/MHz
Isolation		From ANT to RX, State 4		48		dB
Input return loss	|S11|			10		dB
Output return loss	|S22|			12		dB
Power detector output	VDET	@ No RF		0.003		v
		@ +5 dBm		0.05		v
		@+10 dBm		0.23		v
		@ +28 dBm		1.1		v
Power detector slope	SLOPE	From +10 to +26 dBm		40		mV/dB
Power detector error	ERRDET	From +10 to +26 dBm	-1.5		1.5	dB
Power detector output impedance	ZOUT_DET	RF output = -30 dBm		4K		Ω
Stability	STAB	POUT = +25 dBm, VCC = 5 V, 64 QAM, 6:1 VSWR, all phases	none			
Ruggedness	Ru	Maximum input power, 10:1 mismatch, no permanent damage			10	dBm

Table2. Receive Mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Frequency Range			5.15		5.85	GHz
Gain	G	LNA active		14		dB
		LNA bypass		-9.5		dB
1 dB input compression point	IP1dB	LNA active		2		dBm
		LNA bypass		16		dBm
Gain step				23.5		dB
Gain flatness		Over any 40 MHz	-0.5		0.5	dB
Noise figure	NF			2		dB
Input return loss	|S11|	LNA active		10		dB
		LNA bypass		15		dB
Output return loss	|S22|	LNA active		15		dB
		LNA bypass		11		dB
Third order input intercept point	IIP3			15		dBm
LNA bias current	IDD			30		mA
C0, C1 current				10		μA

6.2. Handling Ratings

Table3. Handling Ratings

Symbol	Parameter	Min	Typ	Max	Units
T_{STG}	Storage temperature range	-60		+150	℃
	MSL(260℃ per JEDEC J-STD-020)		3		
V_{ESD}	Human body model (HBM)		1000		V
	Charged device model (CDM)		1000		V

6.3. Timing Requirements

Table4. Timing Requirements

Parameter	Conditions	Min	Typ	Max	Units
Switching Time	LNA<-> bypass		200		ns
	RX<->TX: From 10%-> 90% power change of rising or falling edge		400		ns

6.4. Control Logic

Table5.Control Logic

Mode	State	C0	C1	PA_EN
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	0	0
WLAN receive bypass mode	3	1	1	0
WLAN transmit (high-linearity mode)	4	0	1	1

7. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table6.Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
DC Supply Voltage (VDD)	-0.3	5	6	V
Control Logic VIH VIL	 1.5 0		 3.6 0.6	 V V
RF Input Power (Pin), CW, 50ohms, T=25℃ （RX、TX、ANT）			10	dBm
Operating Temperature	-40		85	℃

8. Pin Assignments and Description

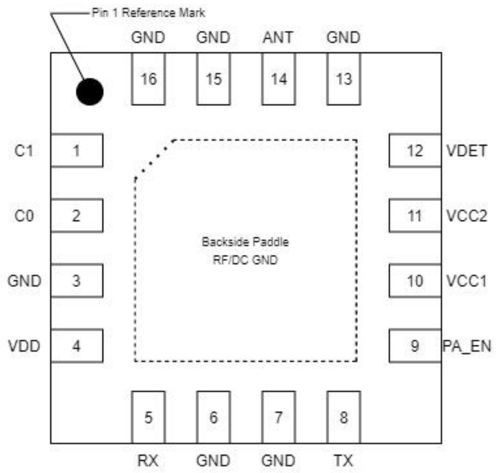


Figure2. Pin Assignments

Table7. Description

Pin No.	Mnemonic	Description
1	C1	Control logic
2	C0	Control logic
3	GND	Ground
4	VDD	LNA supply
5	RX	RF receive output
6	GND	Ground
7	GND	Ground
8	TX	RF transmit input
9	PA_EN	PA enable
10	VCC1	PA supply
11	VCC2	PA supply
12	VDET	Detector output
13	GND	Ground
14	ANT	Antenna
15	GND	Ground
16	GND	Ground

9. Performance Plots

9.1. Transmit-Small signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

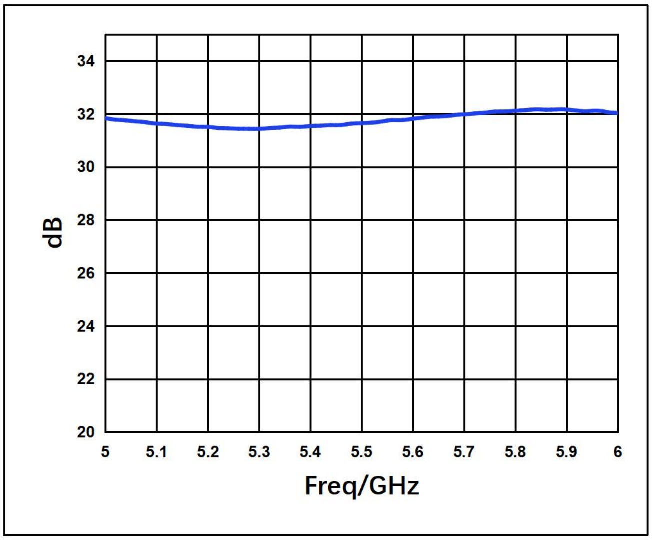


Figure3.Gain vs Frequency

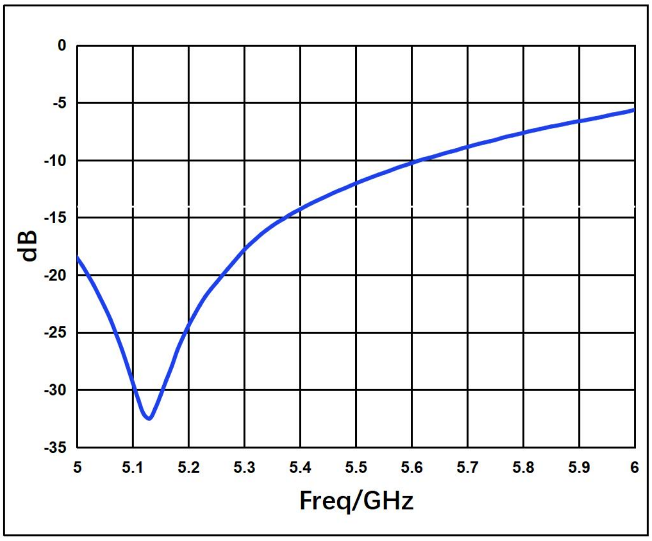


Figure4.Input Return Loss vs Frequency

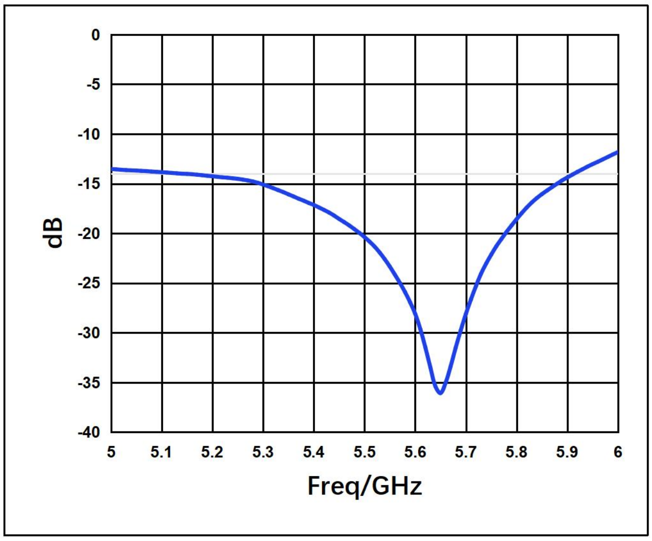


Figure5.Output Return Loss vs Frequency

9.2. Transmit-Large signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

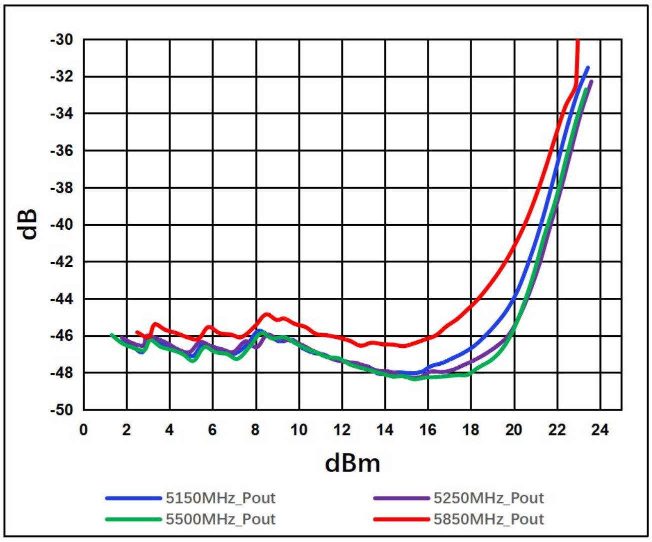


Figure6.EVM vs Pout, HE80

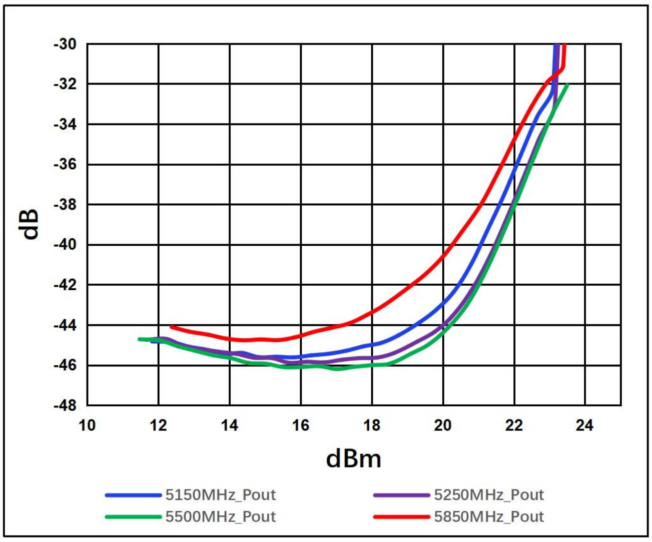


Figure7.EVM vs Pout, HE160

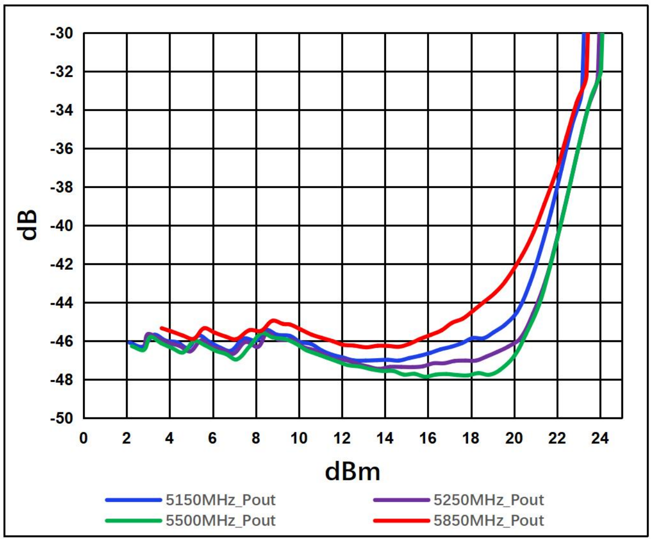


Figure8.DEVM vs Pout, HE80

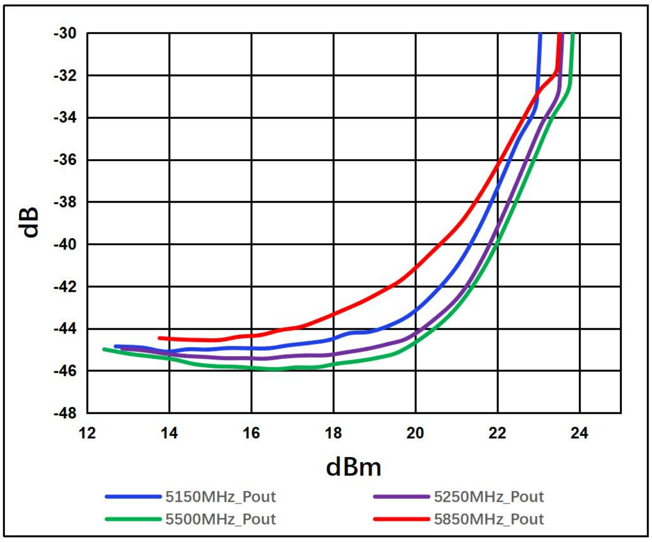


Figure9.DEVM vs Pout, HE160

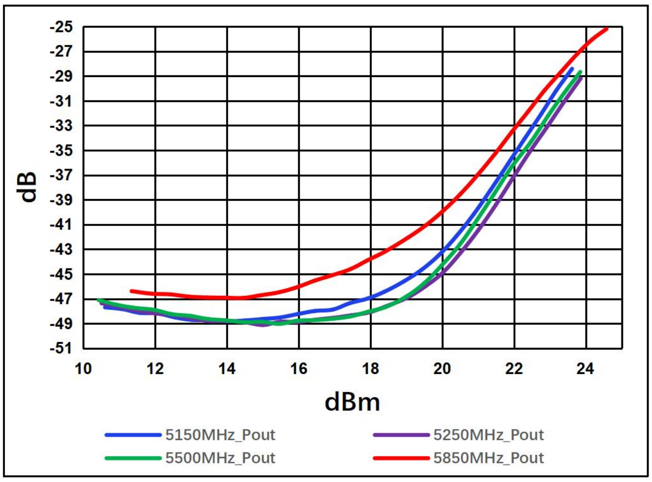


Figure10.EVM vs Pout, VHT80

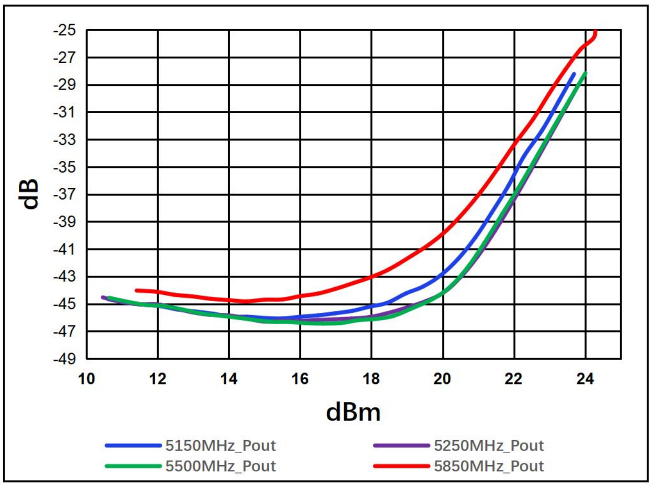


Figure11.EVM vs Pout, VHT160

Transmit-Large signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

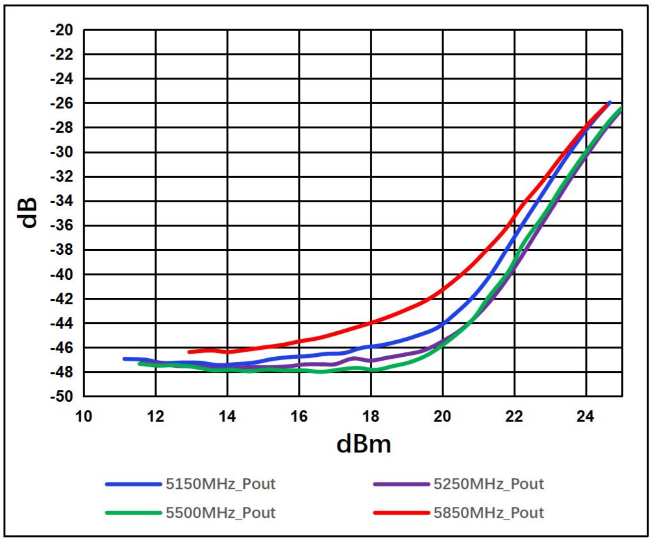


Figure12.DEVM_VHT80

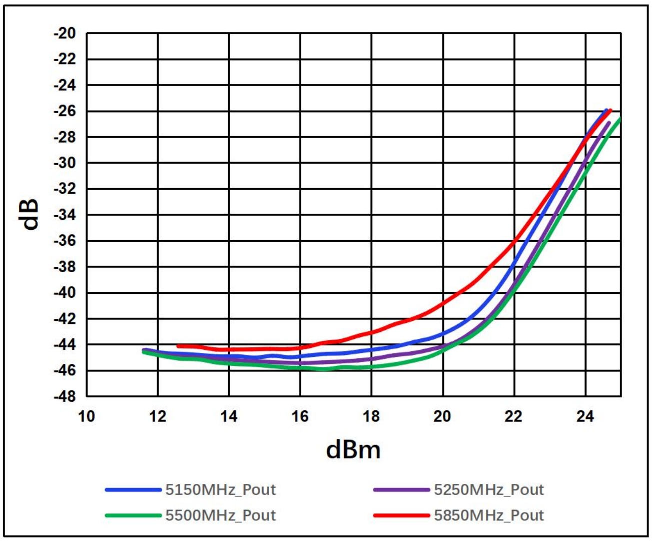


Figure13.DEVM_VHT160

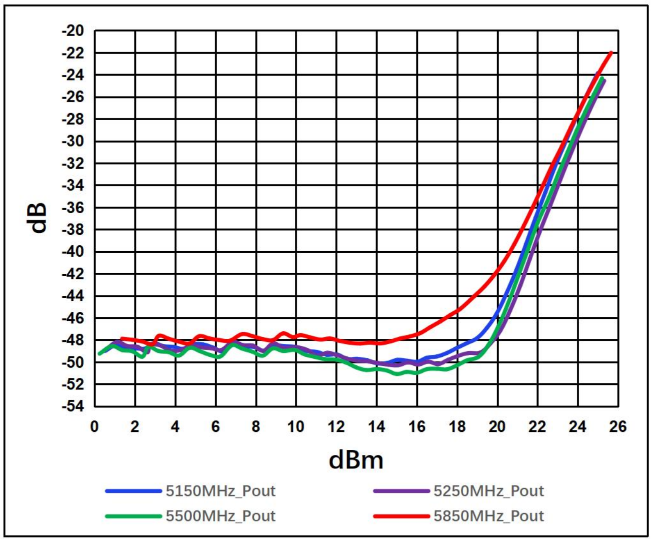


Figure14.EVM vs Pout, HT40

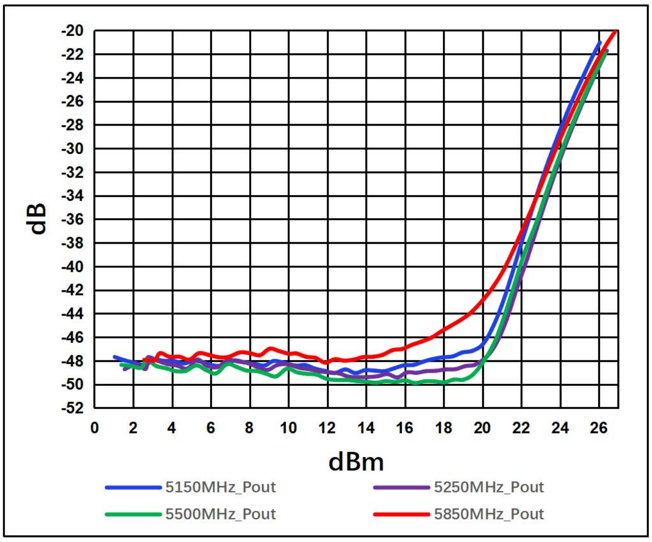


Figure15.DEVM vs Pout, HT40

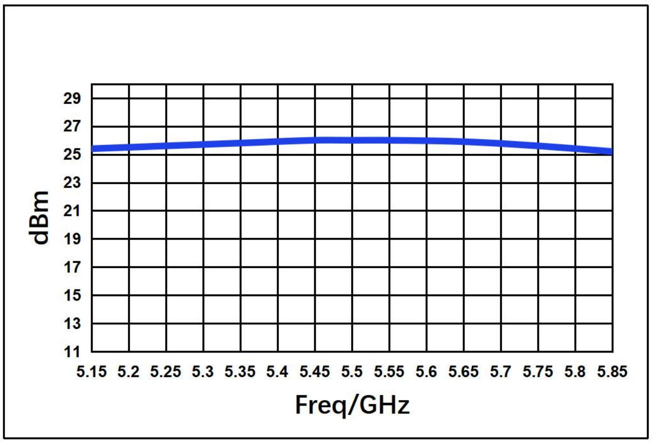


Figure16.Mask vs Frequency ,802.11a

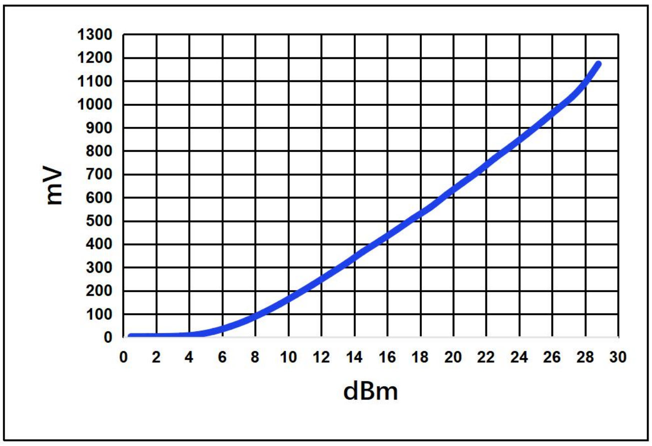


Figure17.Vdet vs Pout

Transmit-Large signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

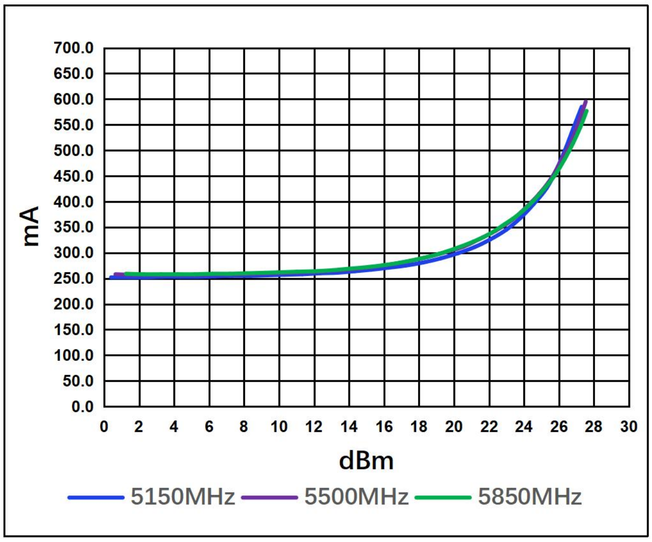


Figure18.Current vs Pout ,802.11a

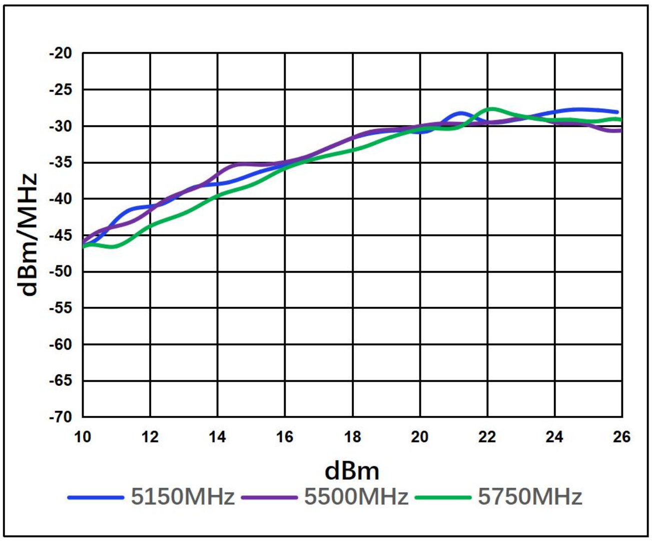


Figure19.2nd Harmonic vs Pout, 802.11a

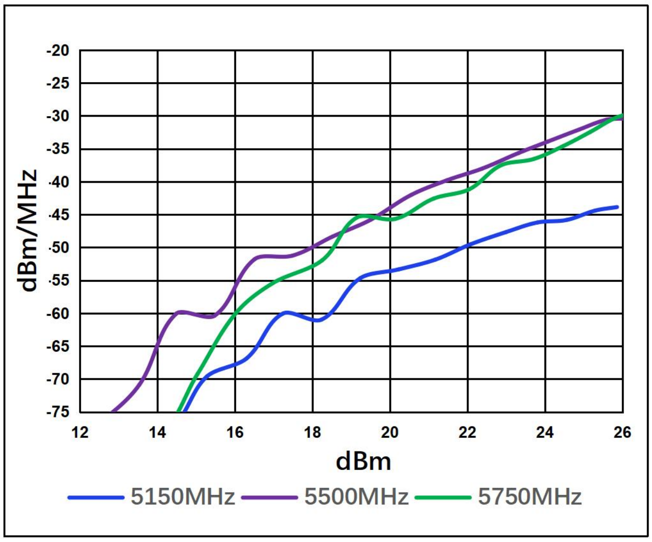


Figure20.3rd Harmonic vs Pout, 802.11a

9.3. Receive-LNA Mode

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

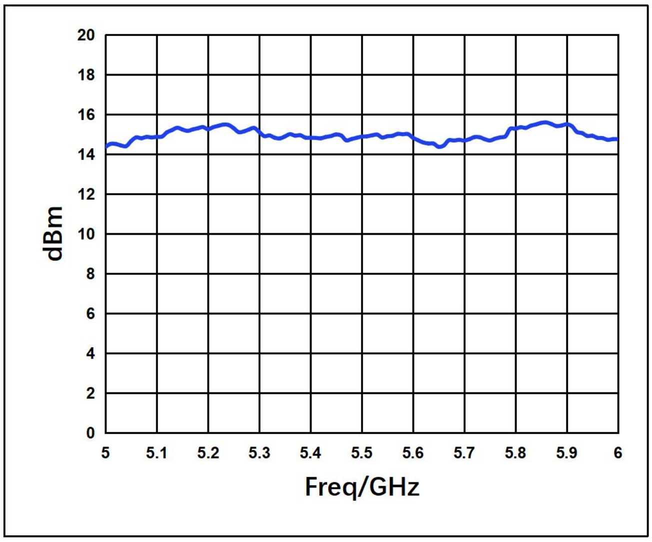


Figure21.LNA_IIP3 vs Frequency

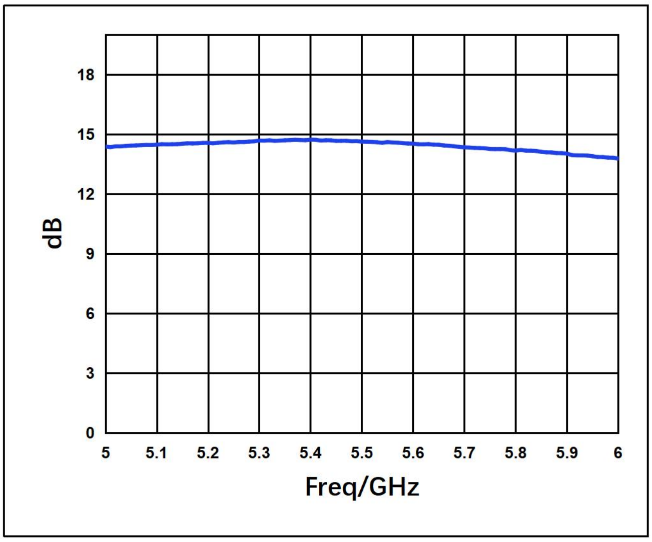


Figure22.LNA_Gain vs Frequency

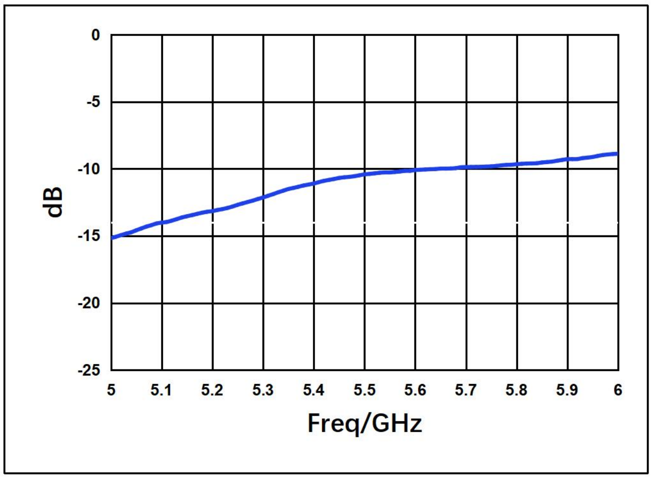


Figure23.LNA_Input Return Loss vs Frequency

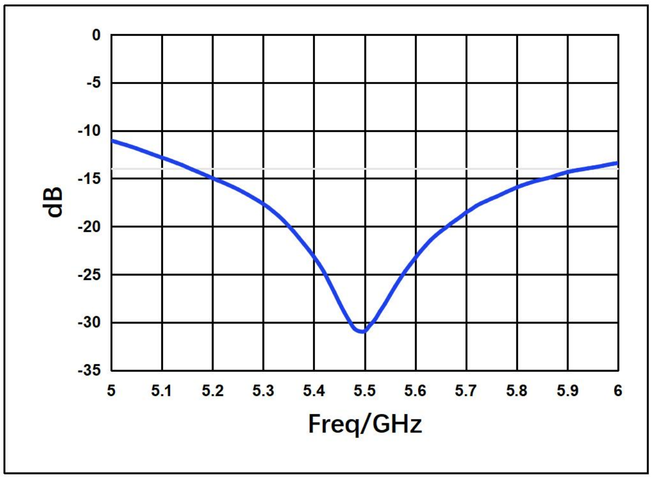


Figure24.LNA_Output Return Loss vs Frequency

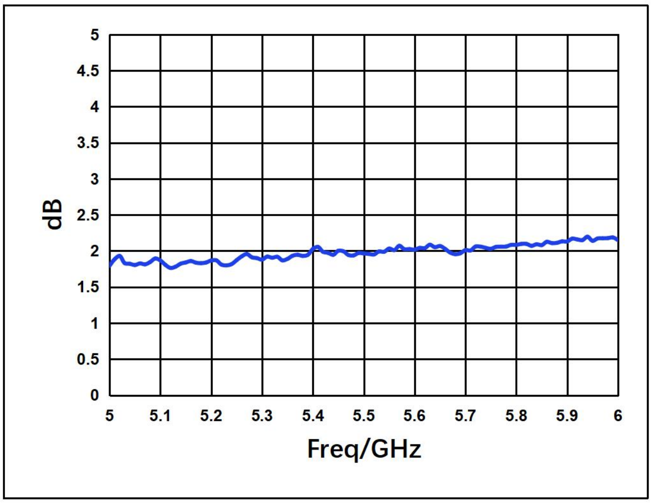


Figure25.LNA_NF vs Frequency

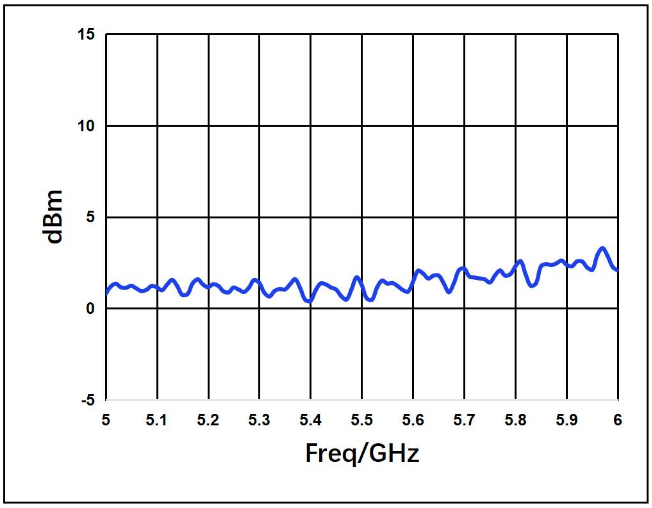


Figure26.LNA_IP1dB vs Frequency

9.4. Receive-Bypass Mode

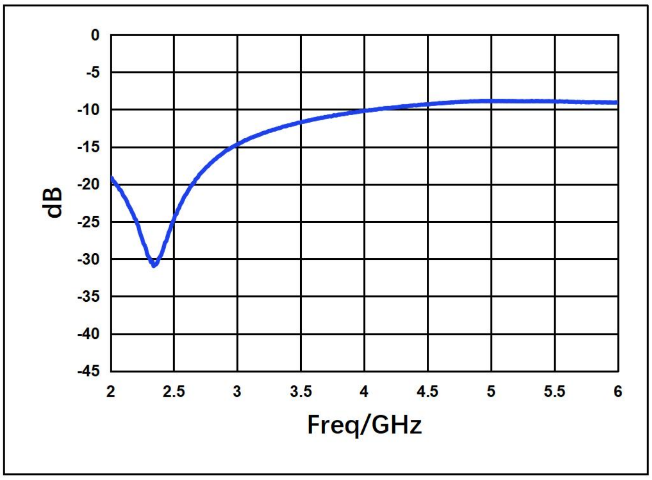


Figure27.Bypass_Insertion Loss vs Frequency (wide band)

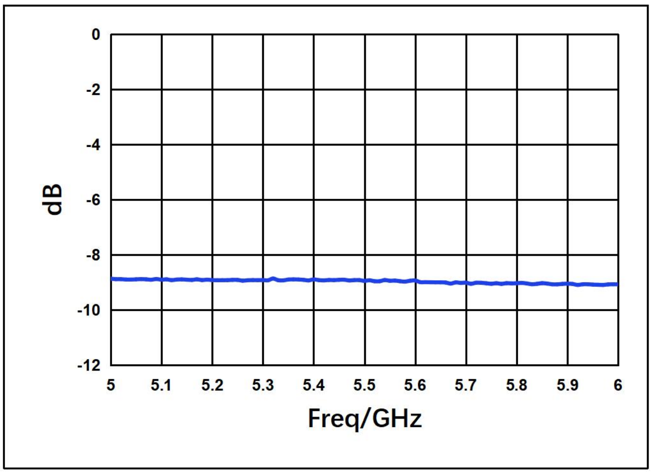


Figure28.Bypass_Insertion Loss vs Frequency

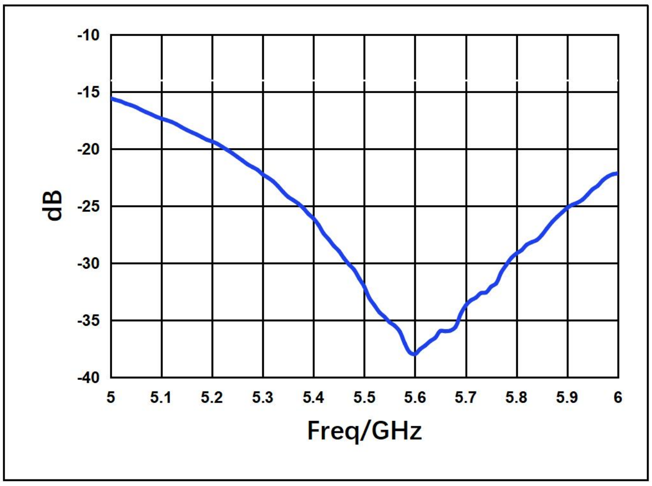


Figure29.Bypass_Input Return Loss vs Frequency

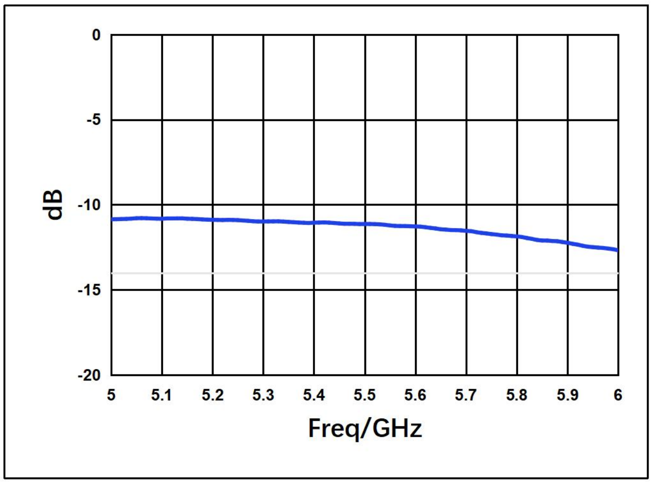


Figure30.Bypass_Output Return Loss vs Frequency

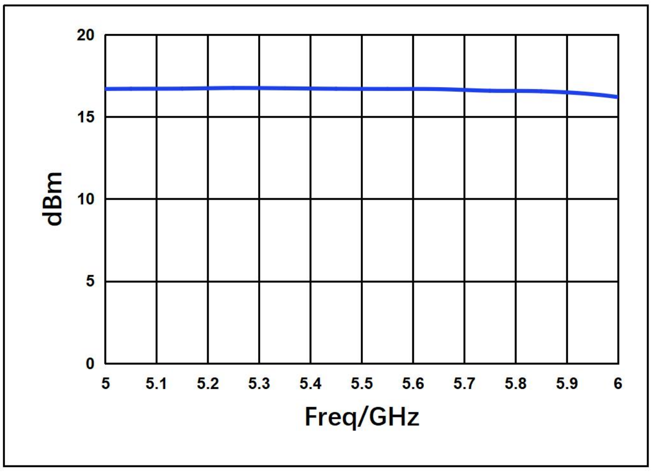


Figure31.Bypass_IP1dB vs Frequency

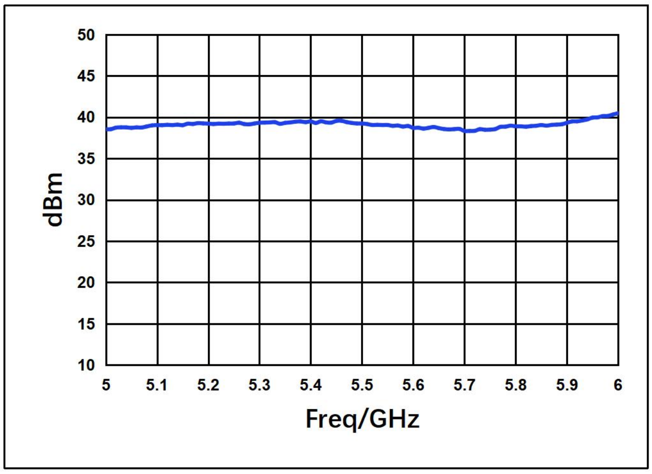


Figure32.Bypass_IIP3 vs Frequency

10. Application

10.1. PCB Evaluation Board

The ARF4501 device is typically placed in a system like the one shown below Figure33.

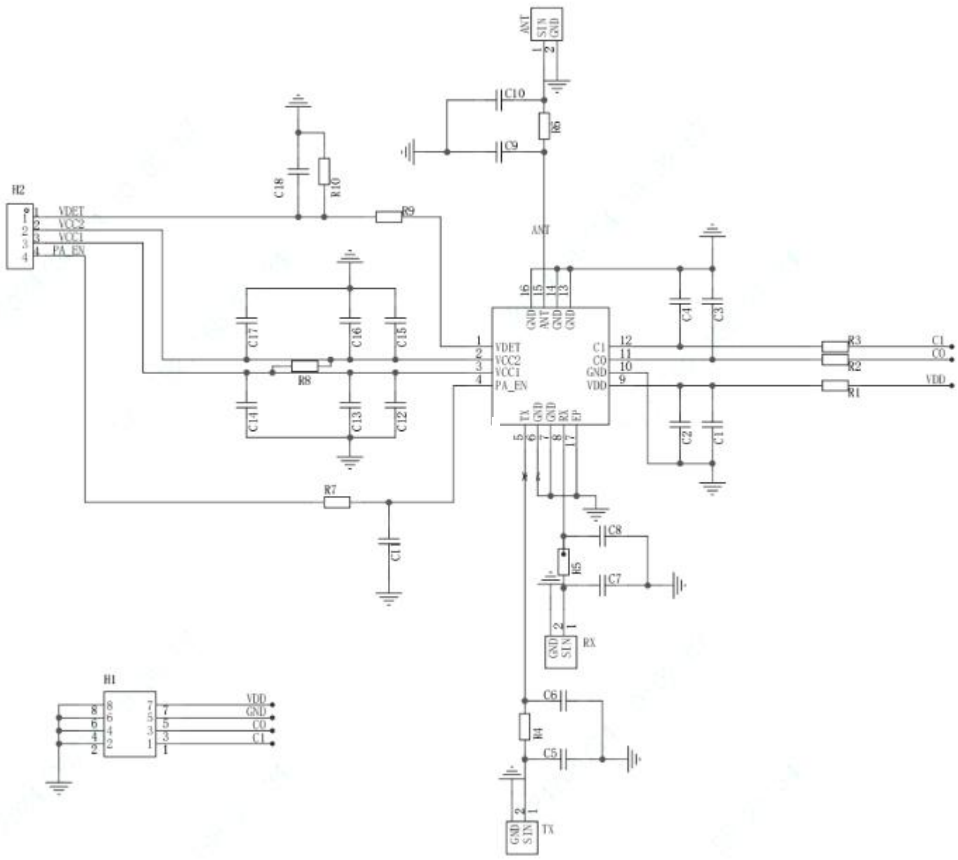


Figure33.

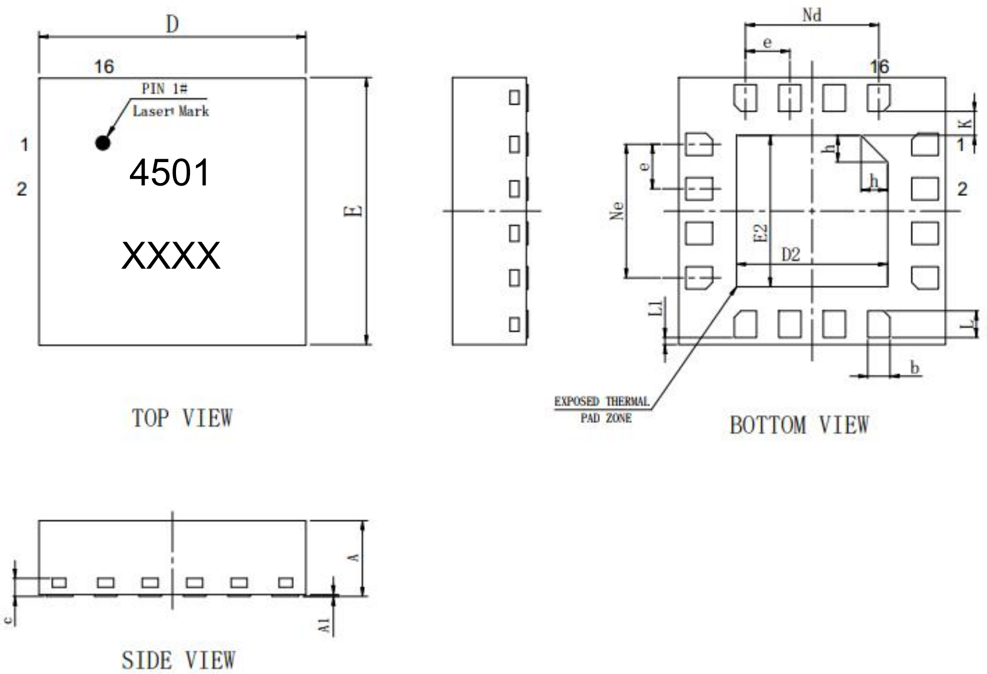
10.2. Evaluation Board BOM

Table8. Bill of Materials for Evaluation PCB

Item	Conditions	Value	Manuf.	Part Num.
C15、C12		220pF	MuRata	0201
C16、C13		2.2uF	MuRata	0201
C2		1nF	MuRata	0201
C3、C4		NA	MuRata	0201
C10		0.3pF	MuRata	0402
C18、C11、C10、C9、C8、C7、C6、C5		NA	MuRata	0402
C1、C14、C17		10uF	MuRata	0603
R10、R8		NA	MuRata	0402
R9、R7、R6、R5、R4、R3、R2、R1		0R	MuRata	0402

11. Package Marking and Outline Dimensions

1) All dimensions are in millimeters.
2) QFN 16 pin 3x3x0.85mm Package.
3) Marking: Part number - 4501
   Lot code - XXXX
4) Coplanarity applies to the exposed heat sink slug as well as the terminals.
5) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 80	0.85	0. 90
A1	0	0.02	0. 05
b	0.20	0.25	0. 30
c	0.203REF		
D	2. 90	3. 00	3. 10
D2	1. 60	1. 70	1. 80
e	0. 50BSC		
Nd	1. 50BSC		
Ne	1. 50BSC		
E	2. 90	3. 00	3. 10
E2	1. 60	1. 70	1. 80
L	0. 25	0. 30	0. 35
h	0. 25	0. 30	0. 35
K	0. 27REF		
L1	0. 08REF		

Figure34. Package Marking and Outline Dimensions

12. Notice

12.1. Operating protection condition

Devices and circuit boards may be undetected. Although this product has an ESD protection circuit, the device may be damaged when encountering high energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid deterioration of device performance or loss of function.

12.2. Operate attention

1. Must be placed in a container with electrostatic protection function, dry environment, conditions permit the best storage nitrogen environment.
2. Please strictly comply with the ESD protection requirements to avoid electrostatic damage.
3. Use vacuum clamps or tweezers to avoid tools or fingers touching the product surface.

12.3. Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

12.4. RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

12.5. Contact Information

Telephone：65-31580333 / 65-80673575

Email：sales@arf-semi.com

Website：www.arf-semi.com

Address：3E Gambas Crescent Singapore 757033

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