1. General Description

ARF4201 is an integrated high power front end module (FEM) designed for Wi-Fi 6 (802.11ax) systems. The compact form factor and integrated matching minimizes layout area in the application. The ARF4201 port impedance is 50 Ω.

2. Features

5 V Operation

33dB TX Gain

14dB RX Gain

MCS11, +21 dBm, -43 dB EVM

MCS9, +22.5 dBm, -35 dB EVM

MCS7, +23.5 dBm, -30 dB EVM

16Pin 3X3mm QFN Package

Integrated 802.11ax, 2.4 GHz PA, LNA with bypass, and T/R switch

Integrated logarithmic power detector and directional coupler

3. Applications

802.11ax set-top boxes, networking, and personal computer systems

PC cards, PCMCIA cards, mini-cards, and half mini-cards

WLAN enabled wireless video systems

4. Functional Block Diagram

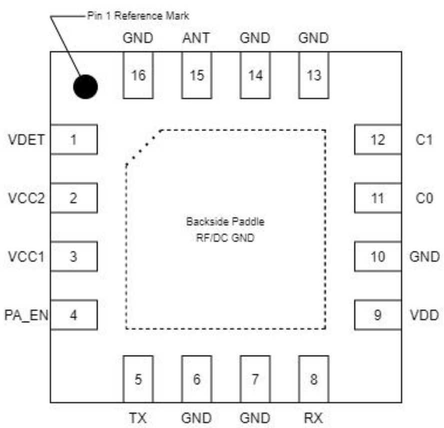


Figure1.

5. Order product model

ARF4201

Directory

6. Specifications

6.1. Electrical Specifications

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

Table1. Transmit Mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Frequency Range			2.4		2.5	GHz
Gain	G		32.6	33	33.4	dB
Gain flatness	ΔG	Over any 40 MHz band	-0.4		0.4	dB
Output power	POUT	DEVM = -43 dB, MCS11, HE40		21		dBm
		DEVM = -40 dB, MCS10, HE40		22		dBm
		DEVM = -35 dB, MCS9, VHT40		22.5		dBm
		DEVM = -30 dB, MCS7, HT20		23.5		dBm
		802.11b, HT20 mask compliant		27		dBm
Current consumption	ITOT	@ +27 dBm		475		mA
		@ +24 dBm		378		mA
		@ +20 dBm		301		mA
		@ +18 dBm		275		mA
2nd harmonics	2fo	+25 dBm MCS0		-11		dBm/MHz
3rd harmonics	3fo	+25 dBm MCS0		-35		dBm/MHz
non-harmonic spurious		+25 dBm MCS0		-50		dBm/MHz
Isolation		From ANT to RX, State 4		50		dB
Input return loss	|S11|			13		dB
Output return loss	|S22|			7		dB
Power detector output	VDET	@ No RF		0.37		v
		@ +5 dBm		0.38		v
		@+11 dBm		0.43		v
		@ +26 dBm		0.75		v
Power detector slope	SLOPE	From +13 to +26 dBm		20		mV/dB
Power detector error	ERRDET	From +13 to +26 dBm	-1.5		1.5	dB
Power detector output impedance	ZOUT_DET	RF output = -30 dBm		10K		Ω
Stability	STAB	POUT = +25 dBm, VCC = 5 V, 64 QAM, 6:1 VSWR, all phases	none			
Ruggedness	Ru	Maximum input power, 10:1 mismatch, no permanent damage			10	dBm

Table2. Receive Mode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Frequency Range			2.4		2.5	GHz
Gain	G	LNA active		14.2		dB
		LNA bypass		-8.6		dB
1 dB input compression point	IP1dB	LNA active		-1		dBm
		LNA bypass		20		dBm
Gain step				22.8		dB
Gain flatness		Over any 40 MHz	-0.1		0.1	dB
Noise figure	NF			1.6		dB
Input return loss	|S11|	LNA active		15		dB
		LNA bypass		15		dB
Output return loss	|S22|	LNA active		12		dB
		LNA bypass		20		dB
Third order input intercept point	IIP3			10		dBm
LNA bias current	IDD			30		mA
C0, C1 current				10		μA

6.2. Handling Ratings

Table3. Handling Ratings

Symbol	Parameter	Min	Typ	Max	Units
T_{STG}	Storage temperature range	-65		+150	℃
	MSL(260℃ per JEDEC J-STD-020)		3		
V_{ESD}	Human body model (HBM)		1000		V
	Charged device model (CDM)		1000		V

6.3. Timing Requirements

Table4.Timing Requirements

Parameter	Conditions	Min	Typ	Max	Units
Switching Time	LNA<-> bypass		200		ns
	RX<->TX: From 10%-> 90% power change of rising or falling edge		450		ns

6.4. Control Logic

Table5.Timing Requirements

Mode	State	C0	C1	PA_EN
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	0	0
WLAN receive bypass mode	3	1	1	0
WLAN transmit (high-linearity mode)	4	0	1	1

7. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table6.Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
DC Supply Voltage (VDD)	-0.3	5	6	V
Control Logic VIH VIL	 1.5 0		 3.6 0.6	 V V
DC Control Voltage	0		6	V
RF Input Power (Pin), CW, 50ohms, T=25℃ （RX、TX、ANT）			10	dBm
Operating Temperature	-40		85	℃

8. Pin Assignments and Description

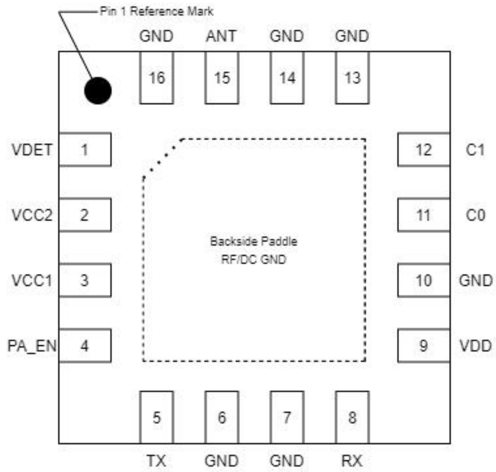


Figure2. Pin Assignments

Table7. Description

Pin No.	Mnemonic	Description
1	VDET	Detector output
2	VCC2	PA supply
3	VCC1	PA supply
4	PA_EN	PA enable
5	TX	RF transmit input
6	GND	Ground
7	GND	Ground
8	RX	RF receive output
9	VDD	LNA supply
10	GND	Ground
11	C0	Control logic
12	C1	Control logic
13	GND	Ground
14	GND	Ground
15	ANT	Antenna
16	GND	Ground

9. Performance Plots

9.1. Transmit-Small signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

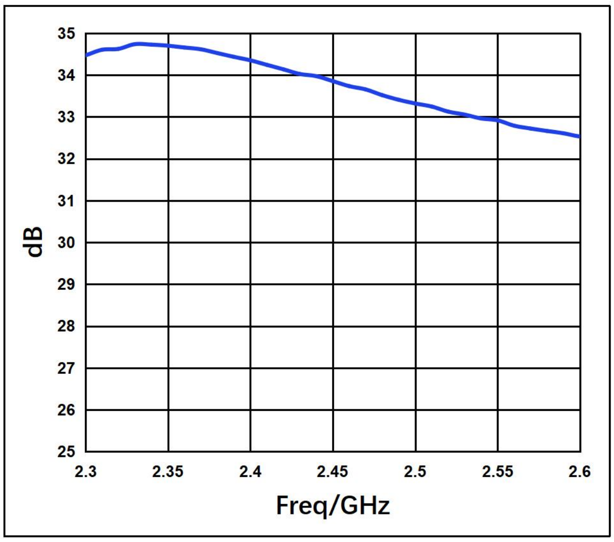


Figure3.Gain vs Frequency

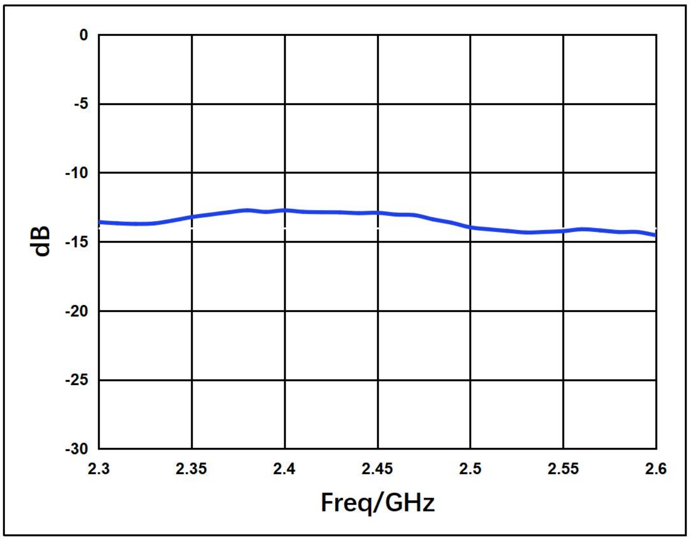


Figure4.Input Return Loss vs Frequency

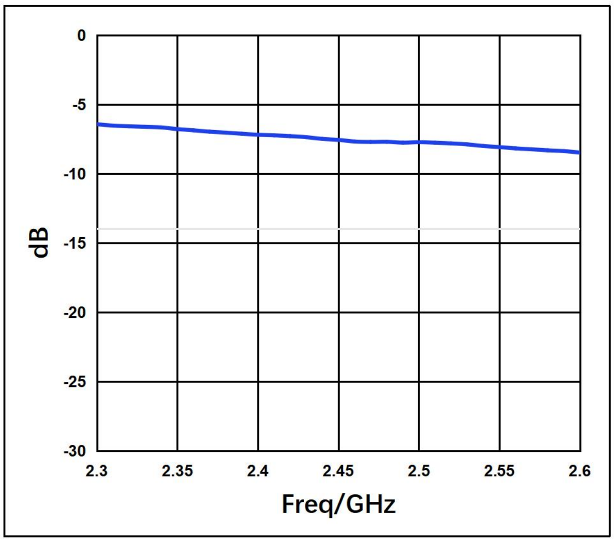


Figure5.Output Return Loss vs Frequency

9.2. Transmit-Large signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

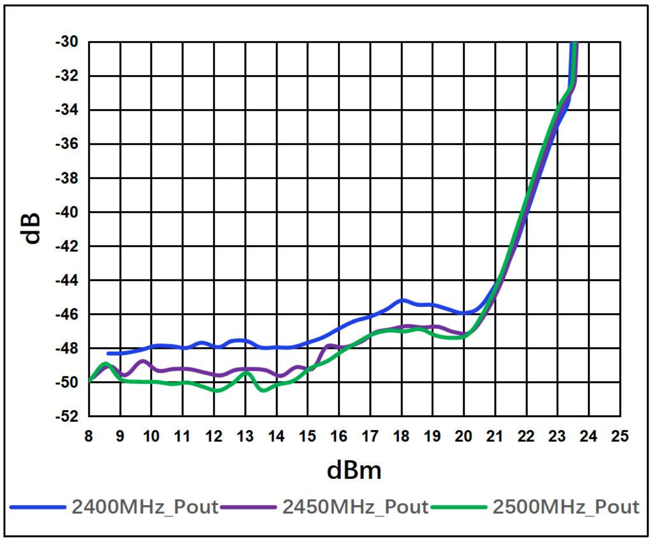


Figure6.EVM vs Pout, HE40

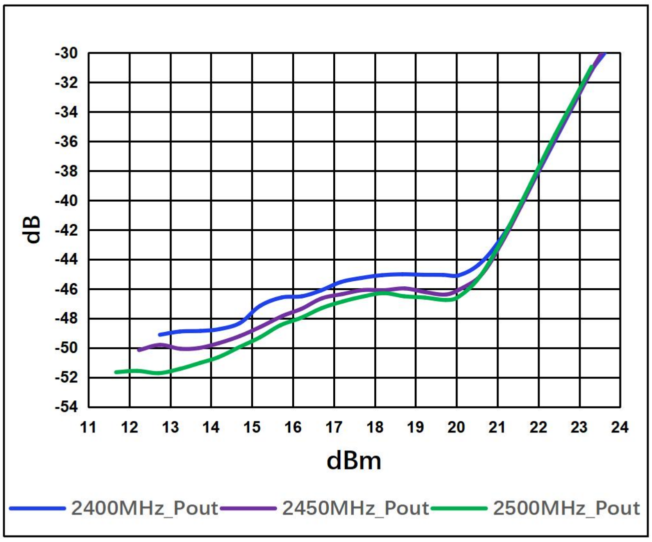


Figure7.EVM vs Pout, VHT40

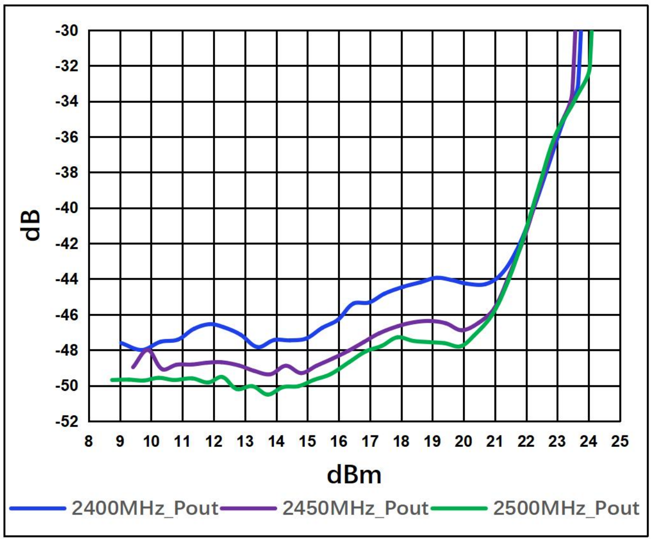


Figure8.DEVM vs Pout, HE40

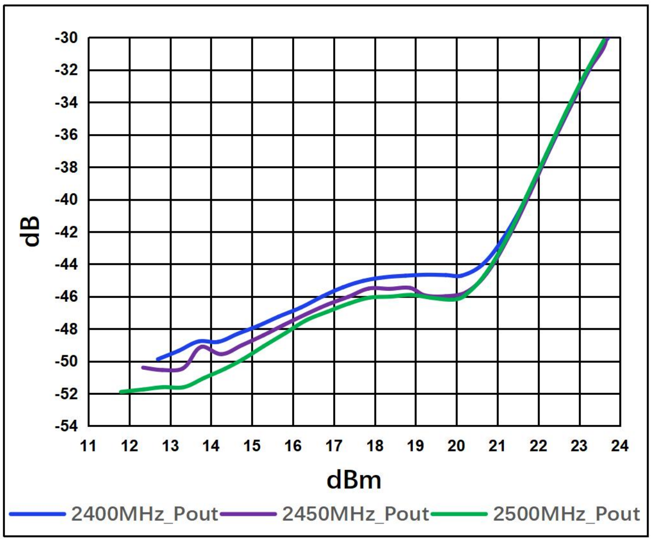


Figure9.DEVM vs Pout, VHT40

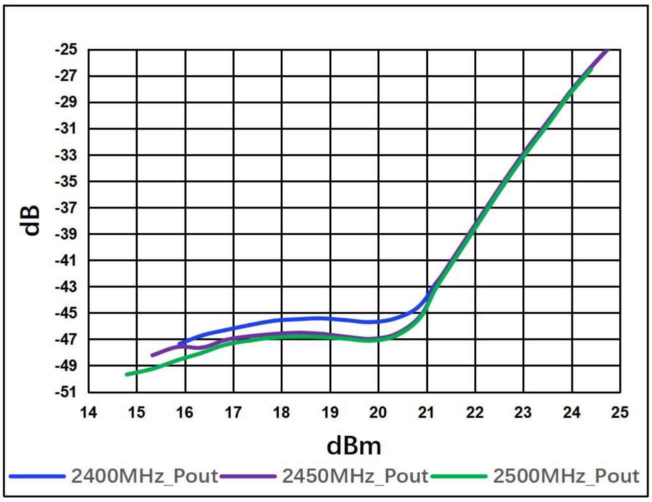


Figure10.EVM vs Pout, HT20

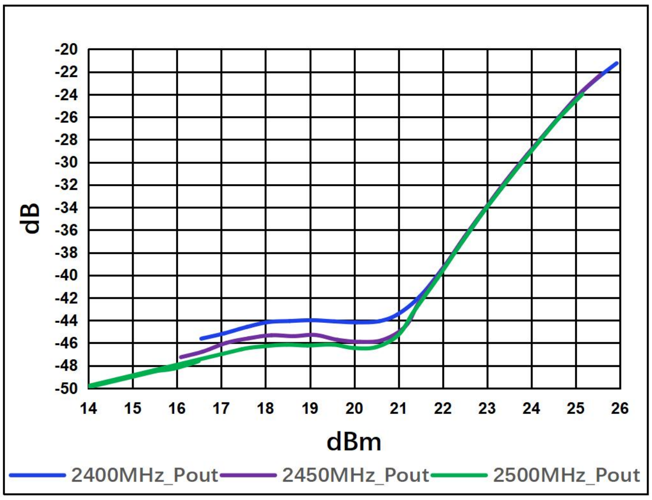


Figure11.DEVM vs Pout, HT20

Transmit-Large signal

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

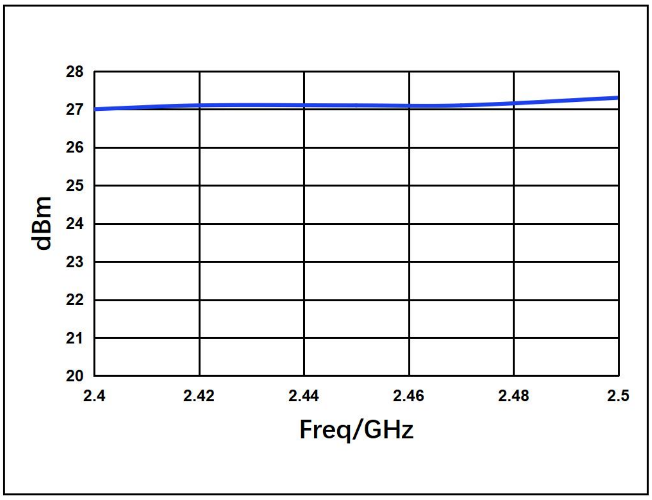


Figure12.Mask vs Frequency 802.11b

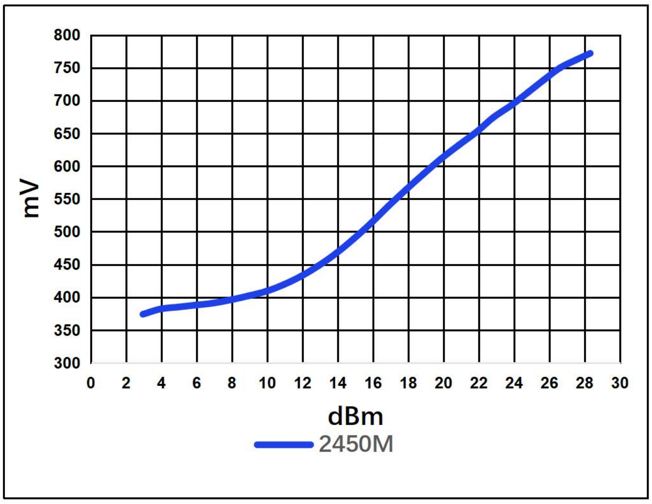


Figure13.Vdet vs Pout

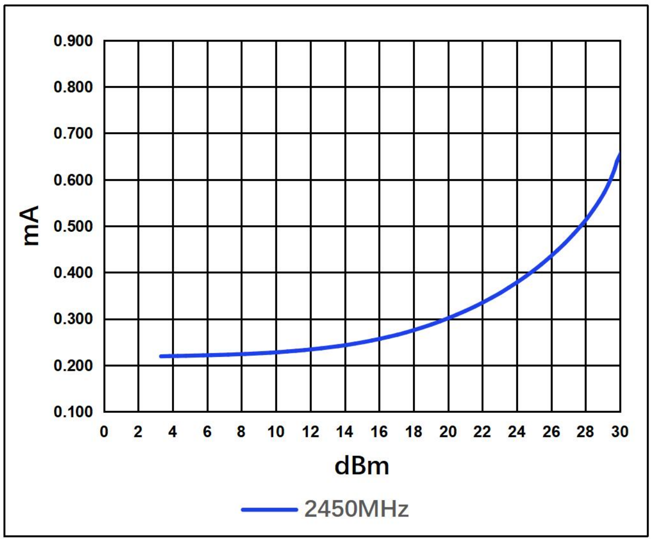


Figure14.Current vs Pout

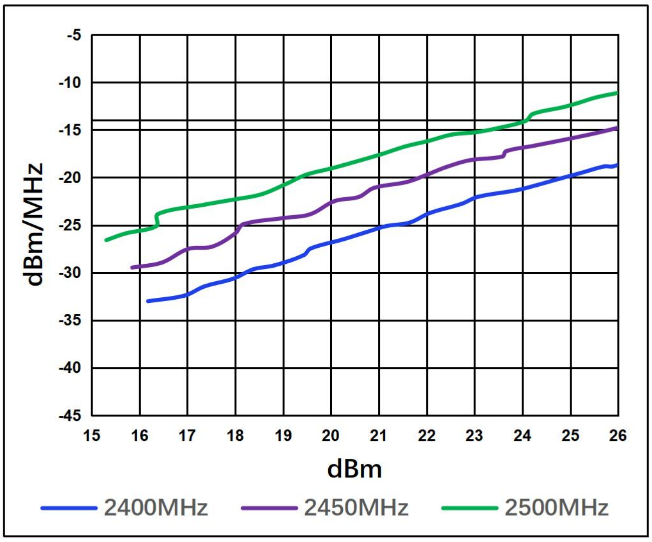


Figure15.2nd Harmonic vs Pout, 802.11b 1 Mbps

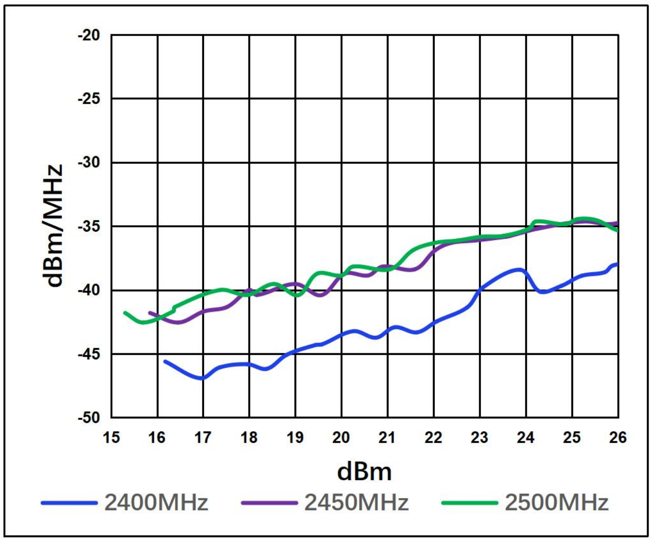


Figure16.3rd Harmonic vs Pout, 802.11b 1 Mbps

9.3. Receive-LNA Mode

Test Conditions: 50Ω system,VCC=VDD=5V, Temp=+25℃, (de-embedded data);

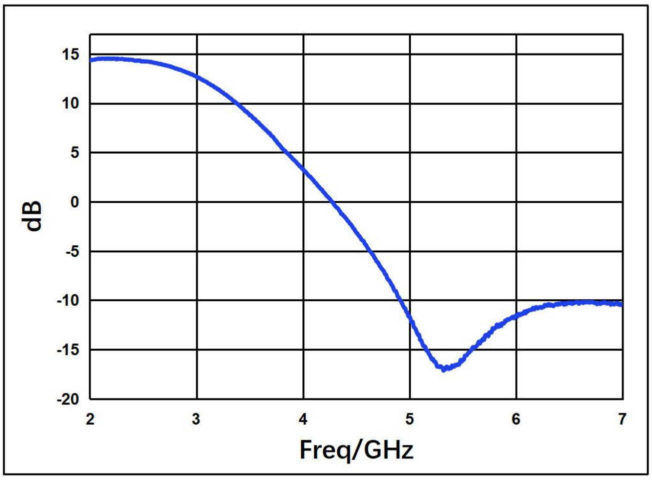


Figure17.LNA_Gain vs Frequency(wide band)

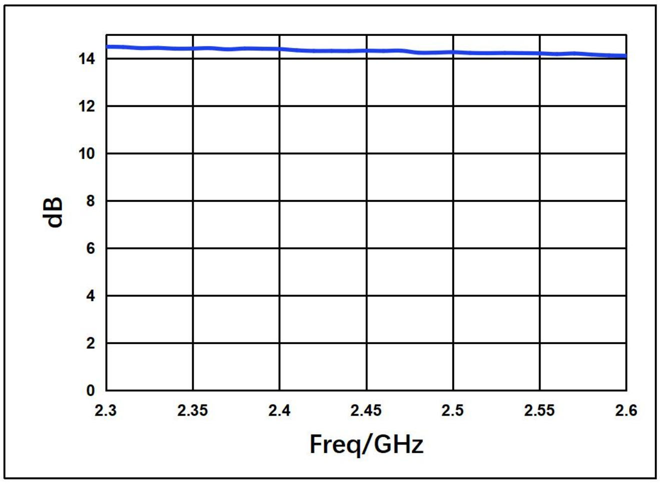


Figure18.LNA_Gain vs Frequency

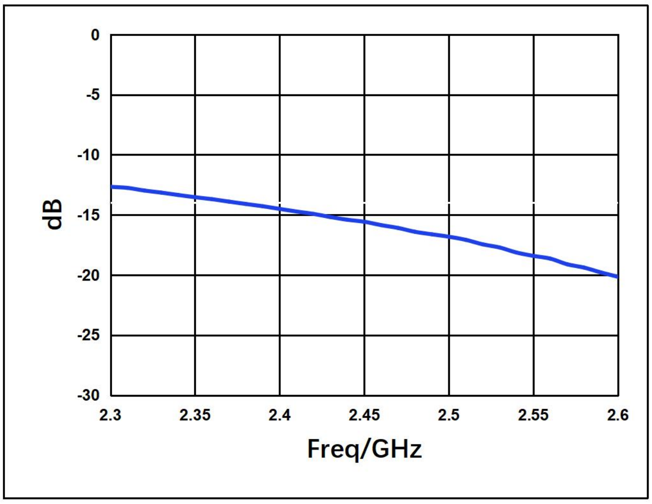


Figure19.LNA_Input Return Loss vs Frequency

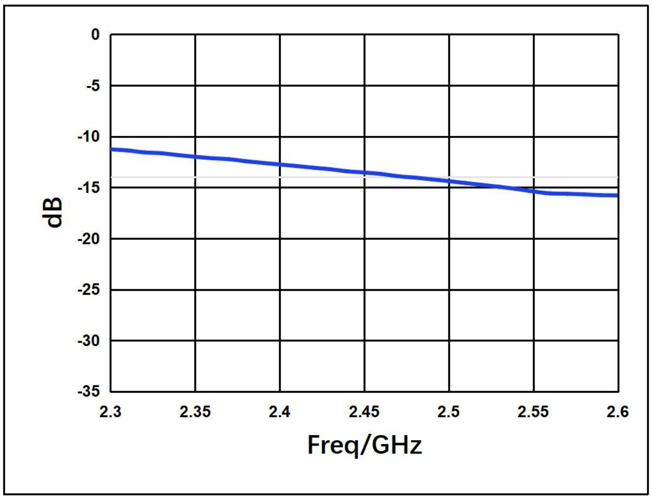


Figure20.LNA_Output Return Loss vs Frequency

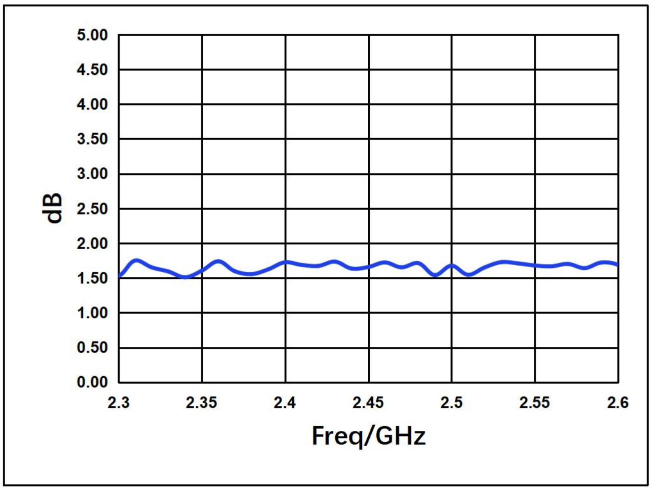


Figure21.LNA_NF vs Frequency

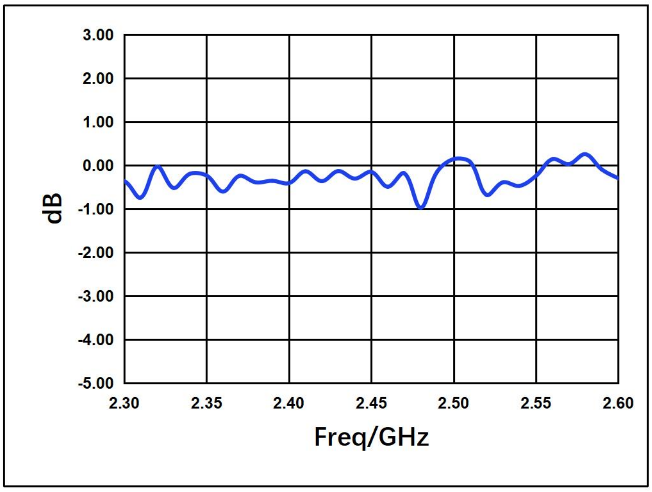


Figure22.LNA_IP1dB vs Frequency

9.4. Receive-Bypass Mode

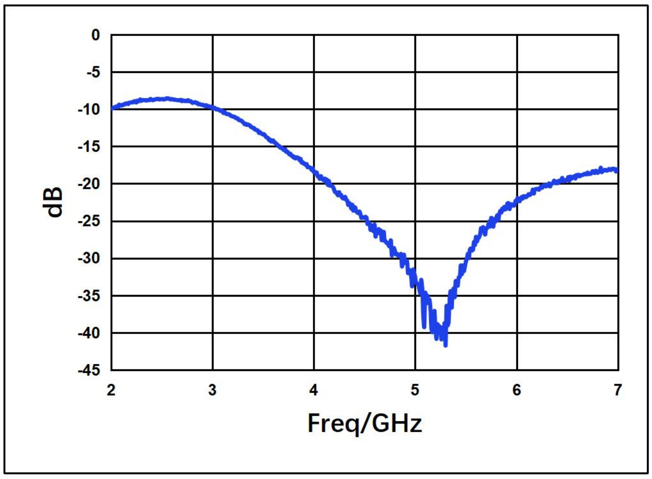


Figure23.Bypass_Insertion Loss vs Frequency (wide band)

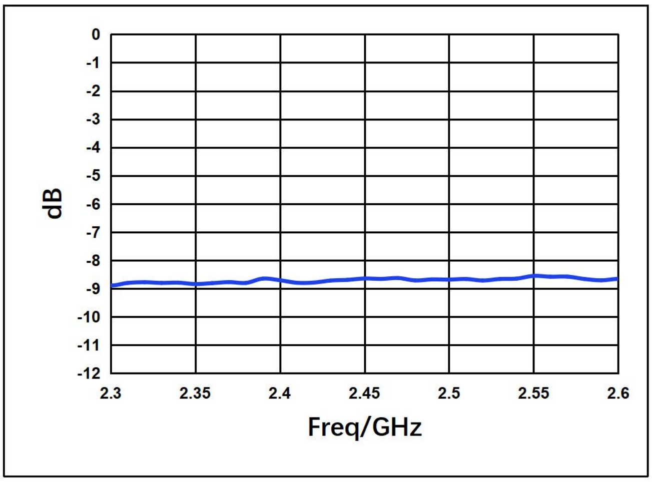


Figure24.Bypass_Insertion Loss vs Frequency

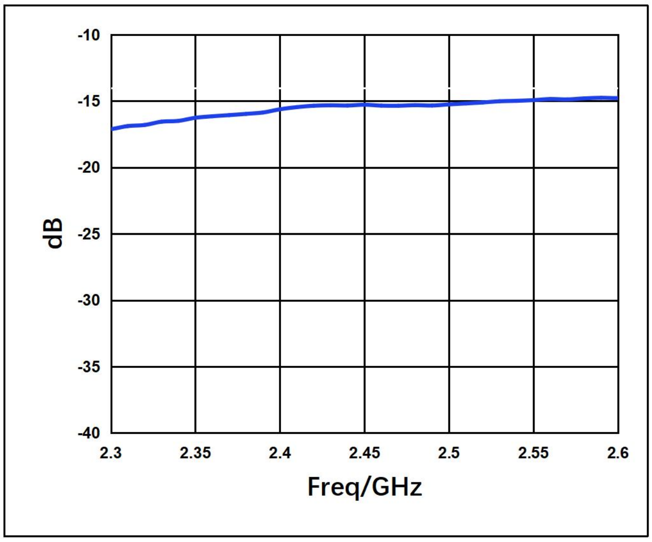


Figure25.Bypass_Input Return Loss vs Frequency

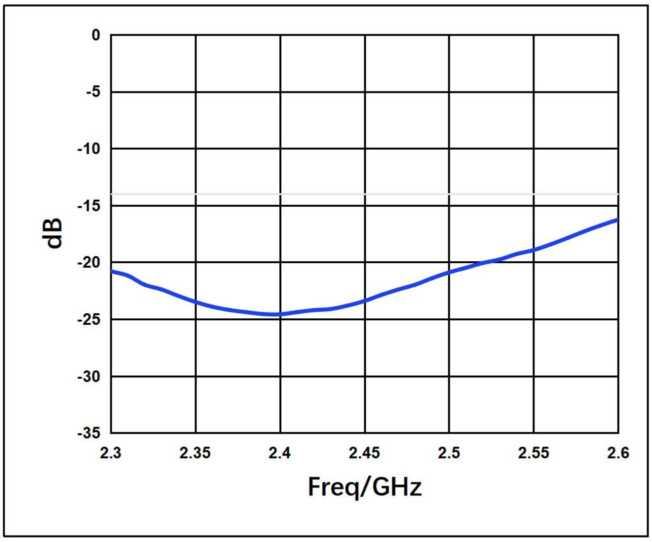


Figure26.Bypass_Output Return Loss vs Frequency

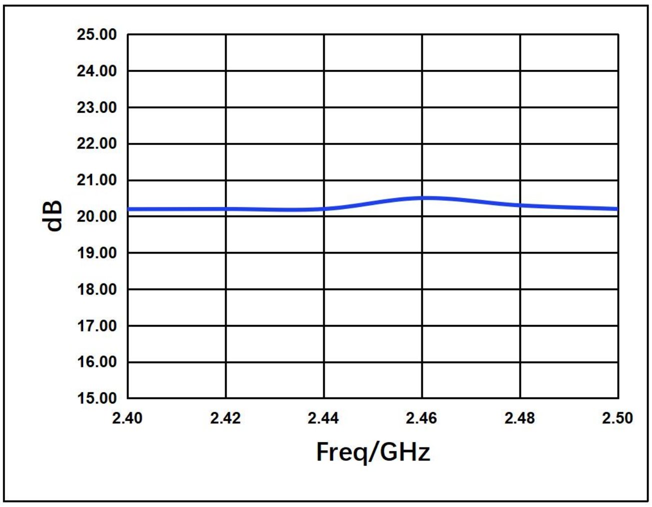


Figure27.Bypass_IP1 vs Frequency

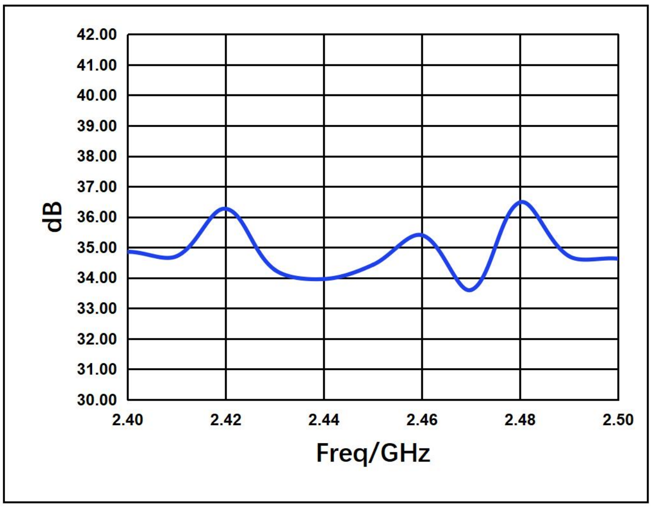


Figure28.Bypass_IIP3 vs Frequency

10. Application

10.1. PCB Evaluation Board

The ARF4201 device is typically placed in a system like the one shown below Figure29.

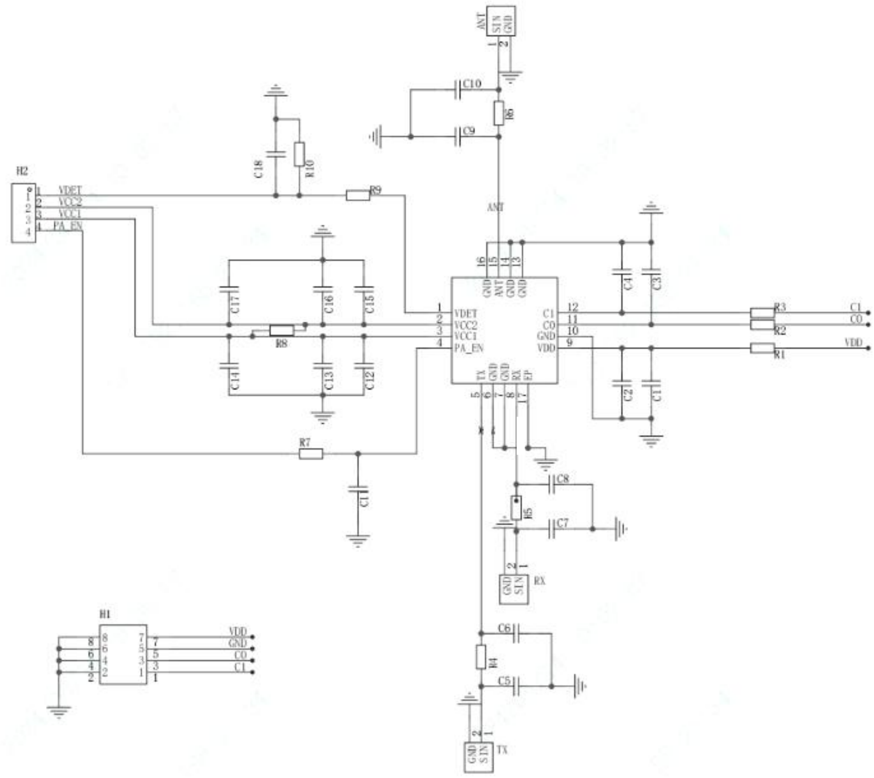


Figure29.

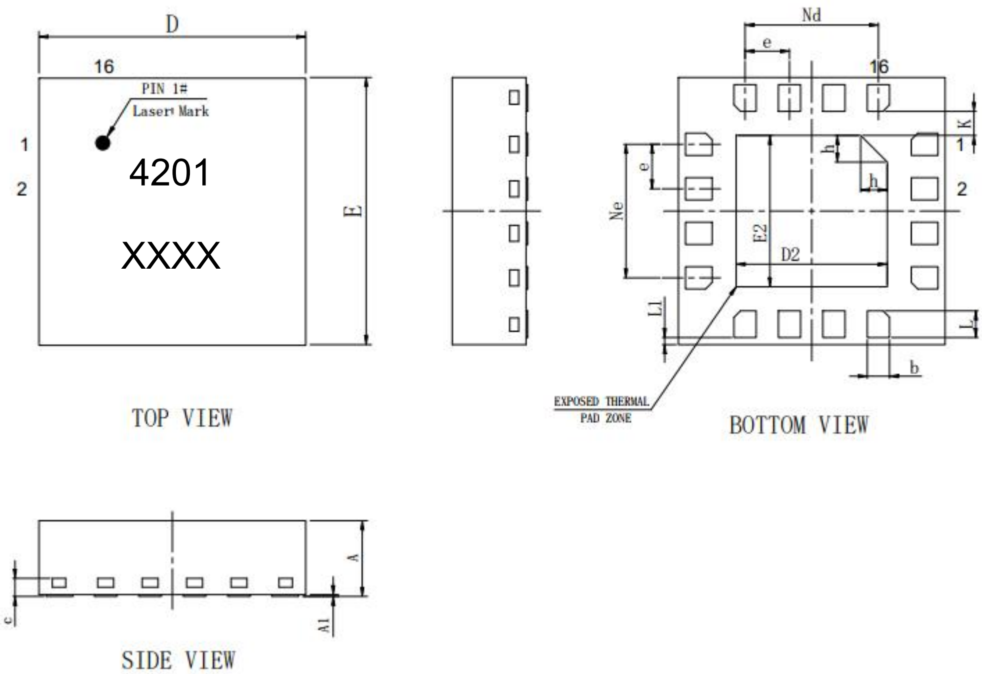
10.2. Evaluation Board BOM

Table8. Bill of Materials for Evaluation PCB

Item	Conditions	Value	Manuf.	Part Num.
C12、C15	N/A	220pF	MuRata	0201
C3、C4	N/A	2.2uF	MuRata	0201
C2	N/A	100pF	MuRata	0201
C5、C6	N/A	300Ω	MuRata	0402
C16、C13	N/A	1nF	MuRata	0201
C18	N/A	100nF	MuRata	0402
C9、C10、C11、C8、C7、R10、R8	N/A	NA	MuRata	N/A
C17、C1、C14	N/A	10uF	MuRata	0603
R4	N/A	16Ω	MuRata	0402
R1、R2、R3、R5、R6、R7、R9	N/A	0R	MuRata	0402
C12、C15	N/A	220pF	MuRata	0201
C3、C4	N/A	2.2uF	MuRata	0201

11. Package Marking and Outline Dimensions

1) All dimensions are in millimeters.
2) QFN 16 pin 3x3x0.85mm Package.
3) Marking: Part number - 4201
   Lot code - XXXX
4) Coplanarity applies to the exposed heat sink slug as well as the terminals.
5) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 80	0.85	0. 90
A1	0	0.02	0. 05
b	0.20	0.25	0. 30
c	0.203REF		
D	2. 90	3. 00	3. 10
D2	1. 60	1. 70	1. 80
e	0. 50BSC		
Nd	1. 50BSC		
Ne	1. 50BSC		
E	2. 90	3. 00	3. 10
E2	1. 60	1. 70	1. 80
L	0. 25	0. 30	0. 35
h	0. 25	0. 30	0. 35
K	0. 27REF		
L1	0. 08REF		

Figure30. Package Marking and Outline Dimensions

12. Notice

12.1. Operating protection condition

Devices and circuit boards may be undetected. Although this product has an ESD protection circuit, the device may be damaged when encountering high energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid deterioration of device performance or loss of function.

12.2. Operate attention

1. Must be placed in a container with electrostatic protection function, dry environment, conditions permit the best storage nitrogen environment.
2. Please strictly comply with the ESD protection requirements to avoid electrostatic damage.
3. Use vacuum clamps or tweezers to avoid tools or fingers touching the product surface.

12.3. Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

12.4. RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

12.5. Contact Information

Telephone：65-31580333 / 65-80673575
Email：sales@arf-semi.com
Website：www.arf-semi.com
Address：3E Gambas Crescent Singapore 757033

Important Notices and disclaimers

The information provided in this document is intended as a guide only and shall not in any event be regarded as a guarantee of conditions, characteristics or performance. ARF does not assume any liability arising out of the application or use of any product described herein, including but not limited to any personal injury, death, or property or environmental damage. No licenses, patent rights, or any other intellectual property rights is granted or conveyed. ARF reserves the right to modify without notice. All rights reserved.

