1. General Description

The ARF1104 is a GaN-on-SiC Power Amplifier operating at 3.4-3.6GHz, power supply +50V operation.

2. Features

Carrier Output Power (P3dB): 40W

Carrier Linear Gain: 20dB

Carrier DE (P3dB): 75 %

Peaker Output Power (P3dB): 70W

Peaker Linear Gain: 19 dB

Peaker DE (P3dB): 72 %

3. Applications

Base station

5G Massive MIMO

WCDMA / LTE

Microcell Base Station

Asymmetric Doherty Applications

Civilian radar

Test instrumentation

4. Functional Block Diagram

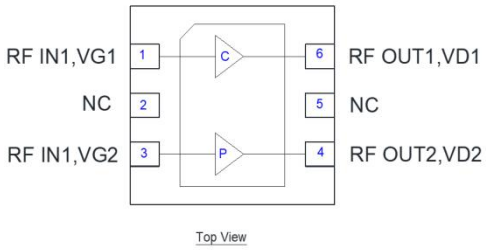

Figure1.

5. Order product model

ARF1104

Directory

6. Specifications

6.1. Electrical Characteristics

Table1. Electrical Characteristics

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Breakdown Voltage						
(main)	V_{GS} = –8 V, I_D = 3 mA	BV_{DG}	V	150	-	-
(peak)	V_{GS} = –8 V, I_D = 6 mA	BV_{DG}	V	150	-	-
Gate Threshold Voltage						
(main)	V_{DS} = 10 V, I_D = 3 mA	V_{GS}(th)	V	-3.4	-2.9	-2.4
(peak)	V_{DS} = 10 V, I_D = 6 mA	V_{GS}(th)	V	-3.4	-2.9	-2.4
Gate Quiescent Voltage	V_{DS} = 50 V, I_D = 65 mA	V_{GS}(Q)	V	-	-2.9	-
Gate-Source Leakage Current						
(main)	V_{GS} = –5 V, V_{DS} = 10 V	I_{Gss}	-	-3.1	-	uA
(peak)	V_{GS} = –5 V, V_{DS} = 10 V	I_{Gss}	-	-6.3	-	uA

6.2. Handling Ratings

Table2. Handling Ratings

Symbol	Parameter	Min	Typ	Max	Units
T_{STG}	Storage temperature range	-65		+150	℃
	MSL		Level 1		
V_{ESD}	Human body model (HBM)		>250		V
	Charged device model (CDM)		>500		V

6.3. Carrier Loadpull Performance

Test conditions: V_D= +50 V, I_{DQ}= 65 mA, Pulsed (10% Duty Cycle, 100 µs Width),Temp = +25 °C.

Table3. Carrier Power Tuned

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	Linear Gain (dB)
3400	15.1-j14.2	6.5-j5.3	46.5	68.6	19.2
3500	20.3-j1.2	6.7-j5.9	46.3	68.0	19.4
3600	15.7+j0.5	6.3-j6.9	46.3	68.0	19.0

Table4. Carrier Effciency Tuned

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	Linear Gain (dB)
3400	20.3-j12.0	5.8+j0.5	45.7	76.0	20.0
3500	12.3-j2.1	5.1-j1.0	45.4	75.9	20.5
3600	10.3-j1.0	5.6-j1.1	45.1	76.3	19.2

6.4. Peaker Loadpull Performance

Test conditions: V_D= +50 V, I_{DQ}=105 mA, Pulsed (10% Duty Cycle, 100 µs Width),Temp = +25 °C.

Table5. Peaker Power Tuned

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	Linear Gain (dB)
3400	15.5-j2.1	4.7-j3.5	48.5	66.0	18.5
3500	12.0+j0.8	4.5-j3.3	48.7	69.4	18.8
3600	5.3-j2.5	4.6-j4.1	48.4	65.0	18.0

Table6. Peaker Effciency Tuned

Frequency (MHz)	Source Impedance (Ω)	Load Impedance (Ω)	P3dB (dBm)	Drain Efficiency (%)	Linear Gain (dB)
3400	12.9+j1.4	3.6-j0.1	47.4	73.9	19.6
3500	6.0+j1.1	3.4-j1.0	47.4	74.3	19.6
3600	3.5-j2.1	3.0-j1.0	46.4	73.0	19.0

6.5. EVB Performance

Table7. EVB Performance

Frequency(MHz)	P3dB (dBm)	Drain Efficiency (%)	Linear Gain (dB)	Units
Frequency	3400	3500	3600	MHz
Linear Gain	16.4	15.5	15.4	dB
Pout@P1dB	45.4	44.5	47.5	dBm
Drain Efficiency@P1dB	58.3	57.5	64.5	%
Pout@P3dB	50.4	50.6	50.4	dBm
Drain Efficiency @P3dB	61.5	62.3	68.4	%

7. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table8. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Gate Voltage Range	-10		1.3	V
Operating Drain Voltage Rang	25		55	V
Max Drain Current (main) (peak)		 3.1 6.3		 A A
Maximum Forward Gate Current (main) (peak)		 4.48 9.2		 mA mA
Operating Environment Temp Range	-40		85	℃
Case Operating Temperature		130		℃
Operating Junction Temperature		225		℃

8. Pin Assignments and Description

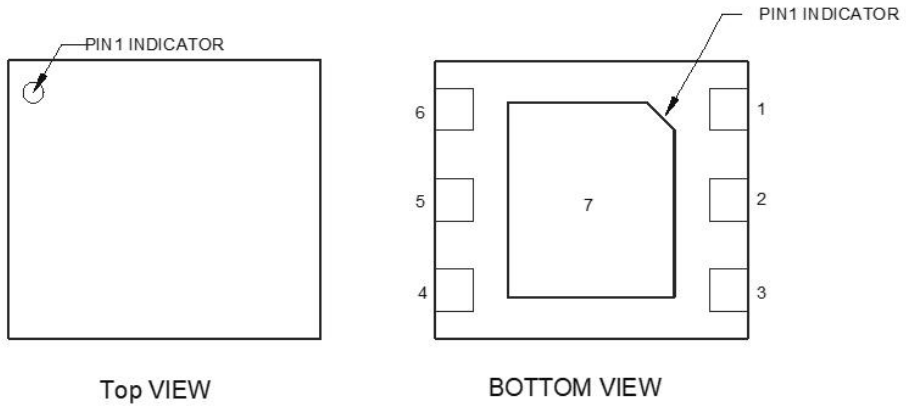

Figure2. Pin Assignments

Table9. Description

Pin No.	Mnemonic	Description
1	RF IN1, VG1	Path 1 RF Input, Gate Bias
2	NC	NC
3	RF IN2, VG2	Path 2 RF Input, Gate Bias
4	RF OUT2, VD2	Path 2 RF Output, Drain Bias
5	NC	NC
6	RF OUT1, VD1	Path 1 RF Output, Drain Bias
7(Back Paddle)	GND	RF and DC Ground

9. Package Marking and Outline Dimensions

1) All dimensions are in millimeters.
2) 6Pin DFN Package.
3) Marking: Part number -1104
   Lot code - XXXX
4) Coplanarity applies to the exposed heat sink slug as well as the terminals.
5) The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

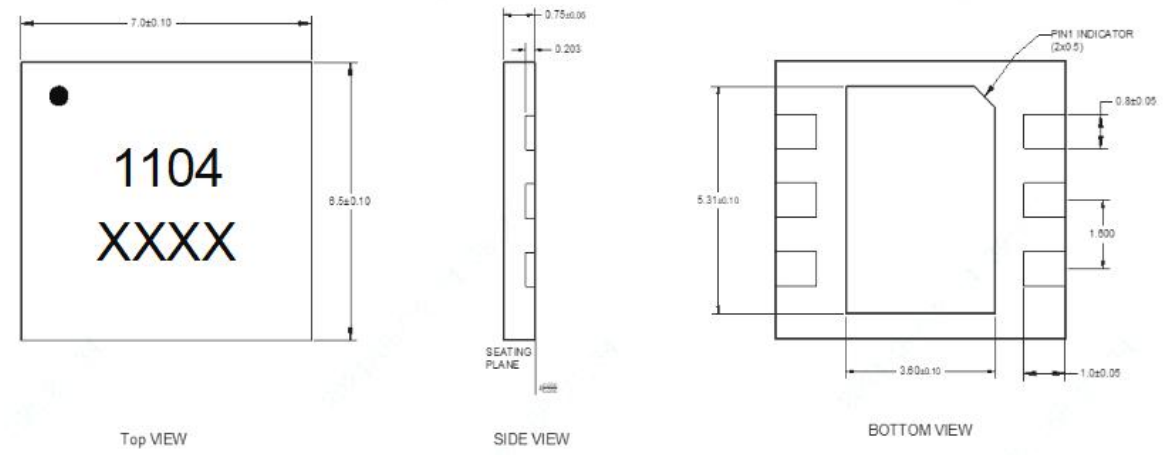

Figure3. Package Marking and Outline Dimensions

10. Notice

10.1. Operating protection condition

Devices and circuit boards may be undetected. Although this product has an ESD protection circuit, the device may be damaged when encountering high energy ESD. Therefore, appropriate ESD prevention measures should be taken to avoid deterioration of device performance or loss of function.

10.2. Operate attention

1. Must be placed in a container with electrostatic protection function, dry environment, conditions permit the best storage nitrogen environment.
2. Please strictly comply with the ESD protection requirements to avoid electrostatic damage.
3. Use vacuum clamps or tweezers to avoid tools or fingers touching the product surface.

10.3. Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

10.4. RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

10.5. Contact Information

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